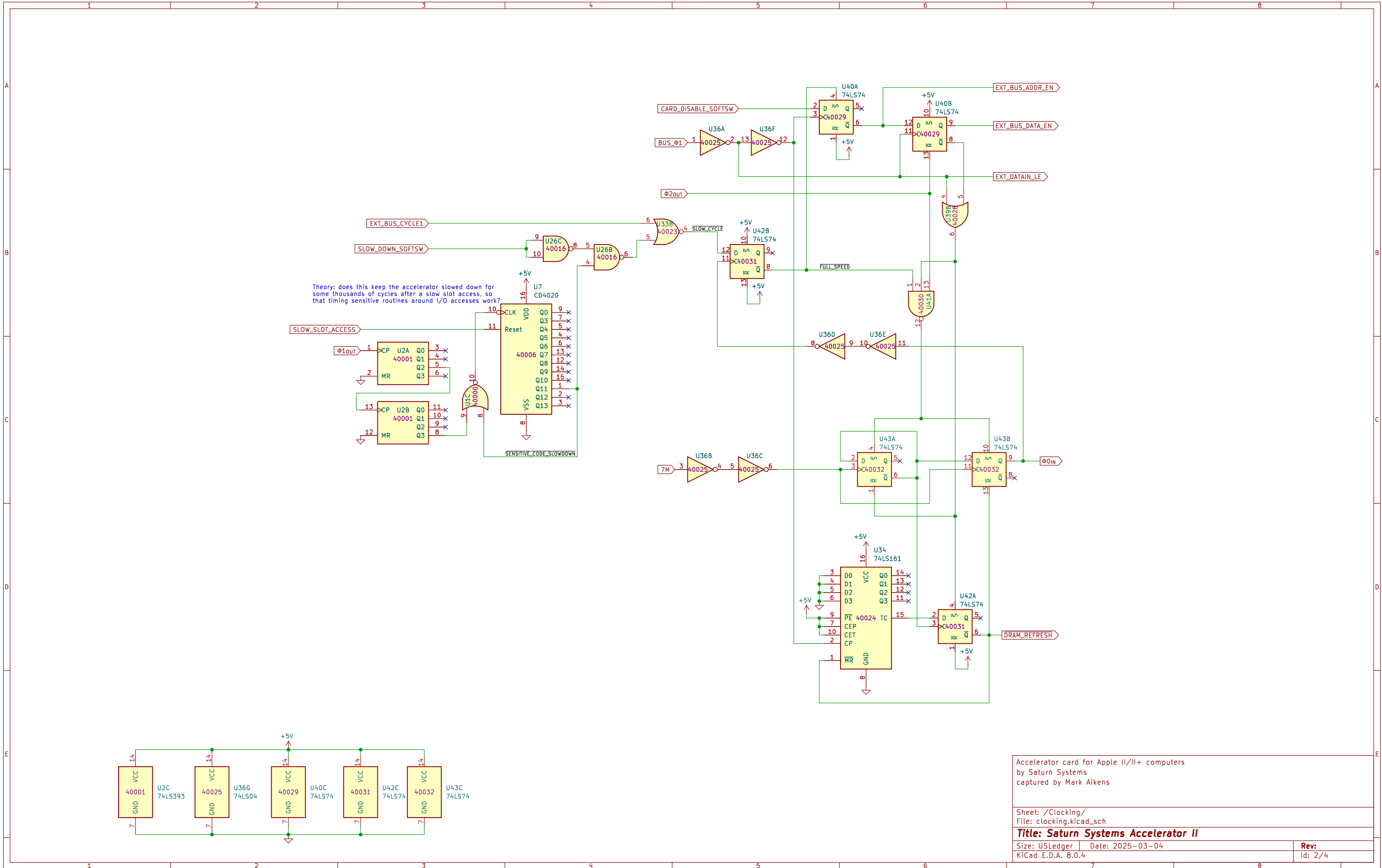


Accelerator card for Apple II/II+ computers
 by Saturn Systems
 captured by Mark Aikens

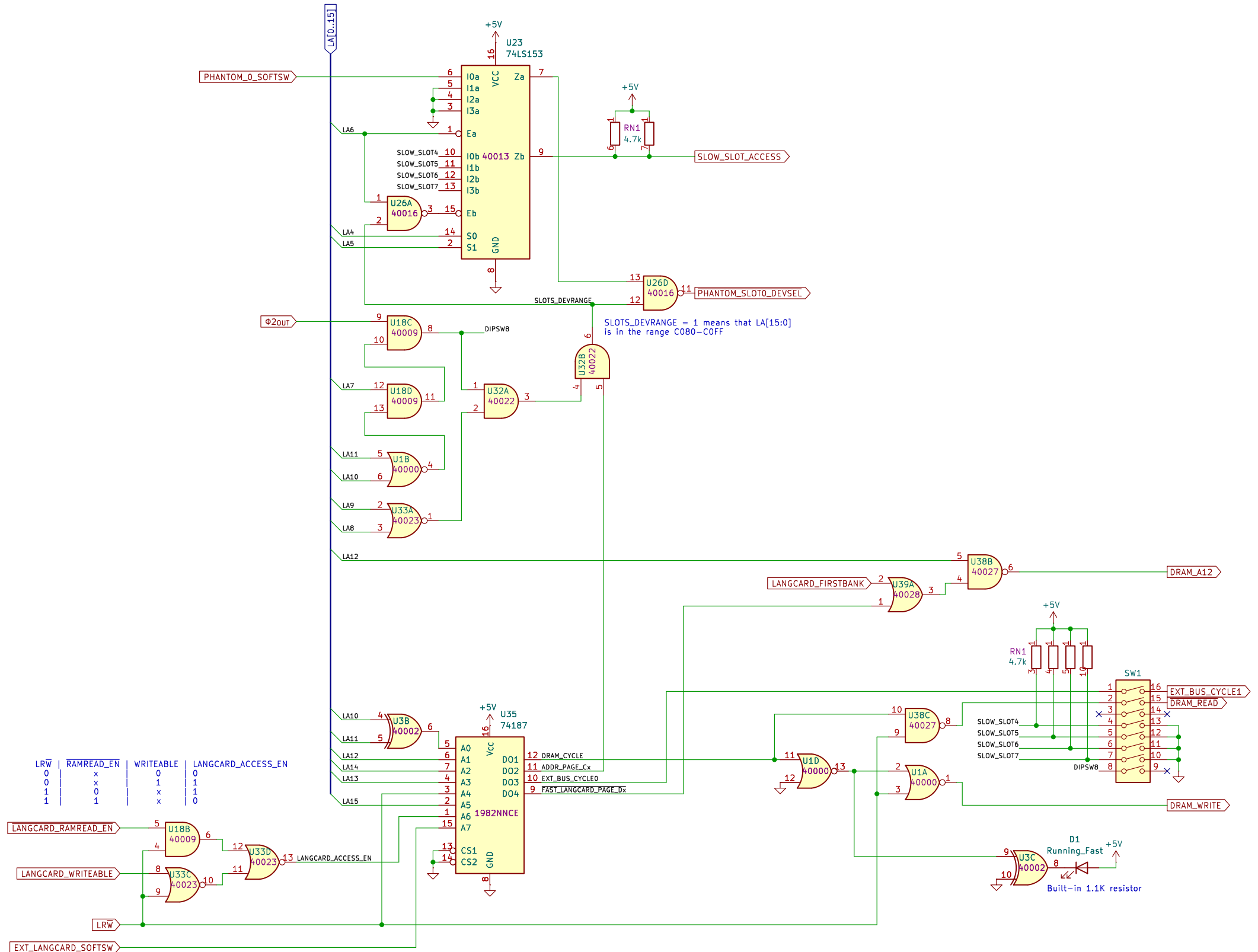
Sheet: /
 File: Saturn-Systems-Accelerator-II.kicad_sch
Title: Saturn Systems Accelerator II

Size: USLedger Date: 2025-03-04 Rev:
 KiCad E.D.A. 8.0.4 Id: 1/4



Theory: does this keep the accelerator slowed down for some thousands of cycles after a slow slot access, so that timing sensitive routines around I/O accesses work?

| | |
|---|------------------|
| Accelerator card for Apple II/II+ computers by Saturn Systems captured by Mark Aikens | |
| Sheet: /Clocking/ File: clocking.kicad_sch | |
| Title: Saturn Systems Accelerator II | |
| Size: USLedger | Date: 2025-03-04 |
| KiCad E.D.A. 8.0.4 | Rev: Id: 2/4 |

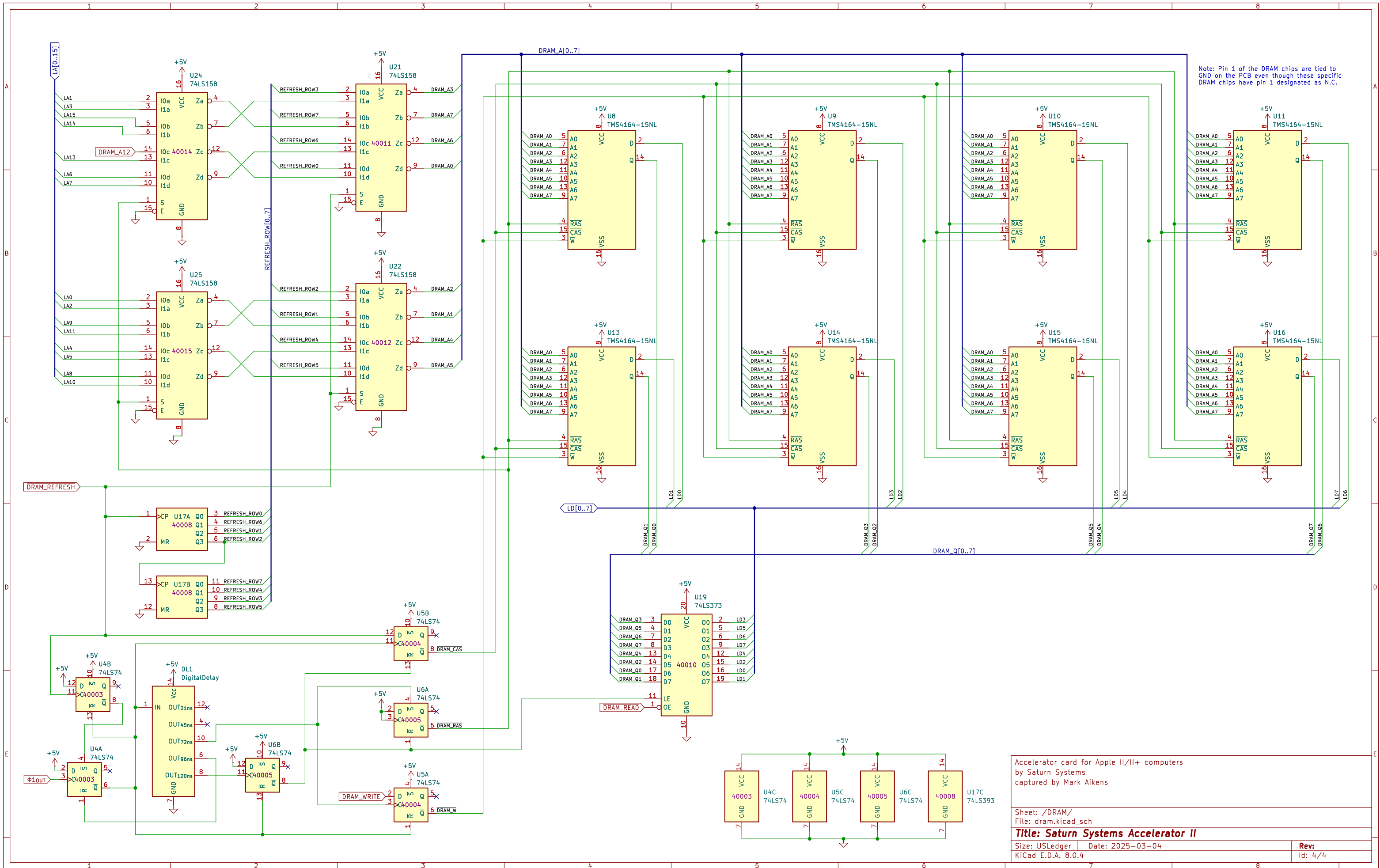


Accelerator card for Apple II/II+ computers
 by Saturn Systems
 captured by Mark Aikens

Sheet: /Address Decoding/
 File: decoding.kicad_sch

Title: Saturn Systems Accelerator II

| | | |
|--------------------|------------------|---------|
| Size: USLedger | Date: 2025-03-04 | Rev: |
| KiCad E.D.A. 8.0.4 | | Id: 3/4 |



Note: Pin 1 of the DRAM chips are tied to GND on the PCB even though these specific DRAM chips have pin 1 designated as N.C.

Accelerator card for Apple II/II+ computers
 by Saturn Systems
 captured by Mark Aikens

Sheet: /DRAM/
 File: dram.kicad_sch

Title: Saturn Systems Accelerator II

Size: USLedger Date: 2025-03-04 Rev:
 KiCad E.D.A. 8.0.4 Id: 4/4