CPU–Complex

File: CPU–Complex.kicad_sch

IO–Ports

File: IO–Ports.kicad_sch

when SELECTED = 1 AND address is in range $8000–$BFFF or $C200–$FFFF then the host is accessing the SRAM or card's internal registers

new values are clocked in at the end of the bus cycle

BUSIN_EN is asserted:
* the bus cycle after a DEVSEL or IOSEL access
* SELECTED is high AND the bus address is in range $8000–$BFFF or $C200–$FFFF

DATA_DIR is 0 (inward) or 1 (outward) from the card's perspective.

When BUSIN_EN is asserted, DATA_DIR=LRW
When BUSIN_EN is not asserted, DATA_DIR=!LRW

is C000–C1FF

is this some sort of I/O trapping mechanism?

TRAP_CYCLE can be asserted on a full address match of any address in C000–C1FF, plus the RW flag.

when BUS_TAKEOVER asserted:
* assert INH
* assert DATA_EN during every PH0
* pull A15 low
* force U27B output to remain high – only allowing wait states to be inserted by DEVSEL and IOSEL accesses

BUS_TAKEOVER theory?

The card traps and overrides an I/O register read access by stopping the host CPU and then running code to place a value on the data bus. During this bus takeover:
* INH is asserted to disable all memories
* A15 is forced low to stop the I/O register from responding to the read
* the card enables the transceiver to connect it's internal data bus to the main bus

LATCHED_CARDSEL is 1 at steady state

when DEVSEL or IOSEL are asserted then the U22B output goes low. This value is latched at the end of the bus cycle and causes the U22B output to return to high

LATCHED_CARDSEL is low throughout the next bus cycle

On the next bus cycle the U22B output will always be high (regardless if any SEL signal is asserted) and then latched at the end of the cycle.

values latched at the end of PH0

SLOW_CYCLE = 1 means that the card is running at half the Apple bus speed. It rises at the end of a Phase 0, one Q3 cycle before LCPUCLK goes high.

Slow cycles are used by the card CPU to synchronize access to the host memory using DMA.

LBUSCLK selection precedence:
* if BUSIN_EN is asserted then LBUSCLK will be Φ0
* if LATCHED_RESET is asserted then LBUSCLK will be Q3
* if LA19 is set then LBUSCLK will only assert during every alternate Φ0 cycle
* else LBUSCLK will be Q3

if LA18 is 0 when SLOW_CYCLE is 1 then the card CPU is accessing host memory

| | |
|---|---|
| G32 Adaptive Firmware Card<br>by Adaptive Peripherals<br>captured by Mark Aikens | |
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| **Title: Adaptive Peripherals G32 Adaptive Firmware Card** | |
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Bus transceivers to connect the local address bus to the main address bus will be enabled if either BUSIN_EN or BUSOUT_EN are asserted.

U24 will not be enabled in the bus cycle after a DEVSEL or IOSEL access and the pullups in RN13 will pull up the lines.

latches top 8 bits of 24-bit address

captures trapped address

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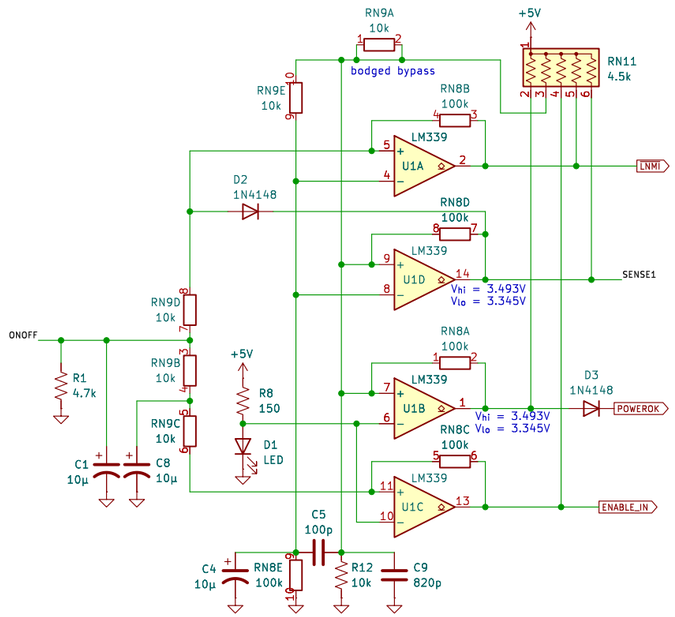


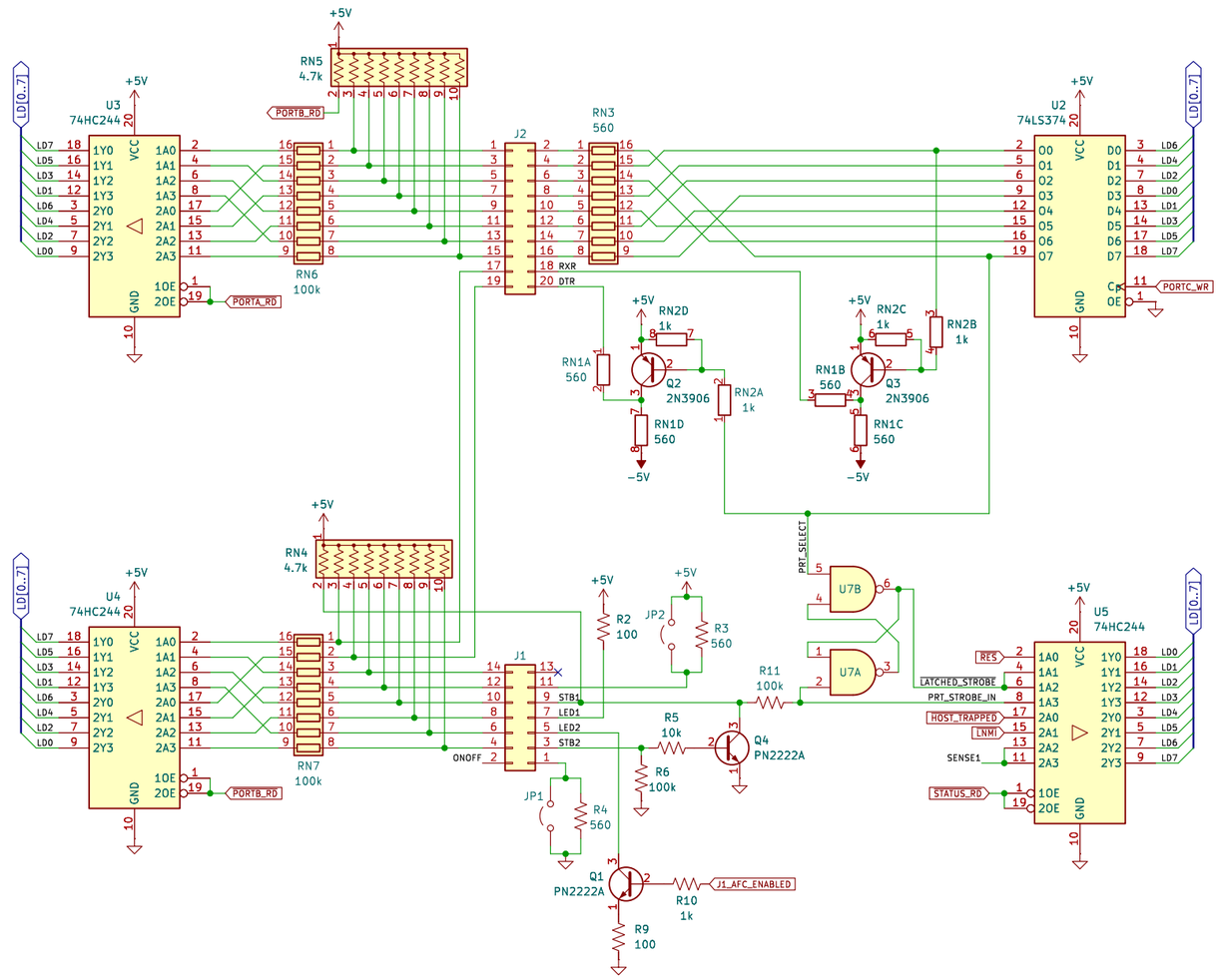




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